REMARKS

Claims 2 – 9, 11 – 18 and 23 – 24 and 26 - 35 are pending. Claims 2, 6, 9, 15, 17, 30 - 32, 34 and 35 are currently amended. Claims 36 – 41 are new. Claims 23, 24, 26 – 29 are currently cancelled and claims 1, 10, 19 – 22 and 25 were previously cancelled. No new matter has been added. Reconsideration is requested.

Applicants would like to thank Examiner Levin for the phone interview on 23 February 2005 with Applicants' representative Suzanne Erez, registration number 46, 688.

CLAIM OBJECTIONS

Claims 23, 24 and 26 – 29 were objected to for being dependent upon a later claim. Claims 23, 24, and 26 – 29 have accordingly been cancelled and reintroduced as new claims 36 – 41.

Claims 6, 15 and 17 were objected to for recitation of the initials AMS. Claims 6, 15 and 17 have been amended accordingly.

Claim 9 was objected to for recitation of the initials. Claim 9 has been amended accordingly.

Claim 32 was objected to for an unclear recitation of "critical interconnect lines" and "transmission line topologies" and the Examiner has requested additional information.

With respect to critical interconnect lines, Applicants respectfully refer to the Specification, page 9, lines 6 – 11 which reads as follows:

> "Some interconnect lines are critical, namely their non-ideal behavior has a large effect on performance, and others may not be. Transmission lines (T-lines) and T-line topologies are inventive, defined, geometric tools that may control the non-ideal behavior properties of the critical interconnect lines and model thereto."

Thus, critical interconnect lines are wires which have non-ideal behaviors that effect performance. Transmission lines are defined, geometric topologies that control the non-ideal behaviors.

The term "transmission lines" is defined in various electrical dictionary and glossaries. The TechFest Network Cabling Glossary (whose website is: www.techfest.com/networking/cabling/cableglos.html), defines them as: "an arrangement of two or more conductors or a wave guide used to transfer a signal from one location to another." A copy of the "T" section of the TechFest Network Cabling Glossary is included herein as Appendix A.

The Innovative Electronics & Computing (IEC) Glossary (www.connectworld.net/iec/Browse02/GLST.html) defines transmission lines as: "An arrangement of two or more conductors or a waveguide used to transfer signal energy from one location to another." A copy of the "T" section from the IEC Glossary is included herein as Appendix B.

While claims 23, 24, and 26 – 29 have been canceled and therefore rejections of these claims are moot, in order to further prosecution, Applicants will respond to such rejections as they concern newly introduced claims 36 – 41.

Luk et al

Claims 2 – 9, 11 – 18, 23 – 24 and 26 – 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Luk et al. (US patent 5,883, 814). Applicants respectfully traverse the Examiner's rejection.

Luk discloses digital technology, as shown by his reference to DRAM and logic in the abstract, in the field of the invention, in column 3, lines 7 – 9 and in Figs. 1 – 14, among other places.

When dealing with wires, digital technology concerns itself with questions of resistance and capacitance, which, together, cause time delays. Thus, digital technology attempts to solve the problems of time delay and does not concern itself with signal integrity.

At low frequencies, inductance effect is limited and has little effect on the digital signal. At high frequencies, the inductance effects distort the signal such that the signal is no longer a pure digital signal but one which also has analog signal characteristics. Hence, those in the art refer to such a signal as an "analog and mixed signal", which acknowledges the fact that the signal has both digital and analog characteristics.

At the high frequencies typical for analog and mixed signals, the inductance corrupts the signal integrity. Thus, systems dealing with analog and mixed signals concern themselves with both time delay and signal integrity. Analog and mixed signal transmission lines are designed to deal with the non-ideal behavior properties of the circuit, e.g. both their time delay and their signal integrity.

Luk, who discloses only digital technology, is concerned only with the time delay caused by a wire, and is not concerned with its signal integrity or inductance. Thus, Luk does not disclose "one or more transmission lines for analog and mixed signal circuit design", as recited in claim 2, or "analog and mixed signal transmission lines" as recited in claim 6, or "an analog and mixed signal integrated circuit" as recited in claims 15, 17, and 30, or "analog and mixed signal transmission line topologies" as recited in claim 31, 32 and 35, or " analog and mixed signal transmission wire models" as recited in claim 34.

Applicants respectfully submit that currently amended claims 2, 6, 15, 17, 30 – 32 and 34 – 35 are allowable over Luk and claims 3 – 5, 7 - 9, 11 – 14, 16, and 18, 33 and claims 36 – 41 dependent therefrom are also allowable over Luk.

Saito et al

Claims 2 – 9, 11 – 18, 23 – 24 and 26 – 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito et al. (US patent application 2002/0095648). Applicants respectfully traverse the Examiner's rejection.

Saito discloses layout methods to prevent noise through a silicon substrate, also known as substrate cross talk. Saito discloses a "method for deciding SUB pin positions where a noise circulation amount is smallest" (paragraph 32). Saito is concerned that "noise caused by the digital circuits affects the analog circuits through the substrate of the LSI" (paragraph 0004). Saito does not discuss or mention transmission lines, much less analog and mixed signal transmission lines.

Thus, Saito does not disclose "one or more transmission lines for analog and mixed signal circuit design", as recited in claim 2, or "analog and mixed signal transmission lines" as recited in claim 6, or "an analog and mixed signal integrated circuit" as recited in claims 15, 17, and 30, or "analog and mixed signal transmission line

topologies" as recited in claim 31, 32 and 35, or " analog and mixed signal transmission wire models" as recited in claim 34.

Applicants respectfully submit that currently amended claims 2, 6, 15, 17, 30 – 32 and 34 – 35 are allowable over Saito and claims 3 – 5, 7 - 9, 11 – 14, 16, and 18, 33 and claims 36 – 41 dependent therefrom, are allowable over Saito.

Chao et al.

Claims 2 - 7, 9, 15 – 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Chao et al. (US patent 5,031,111). Applicants respectfully traverse the Examiner's rejection.

Chao discloses microwave and millimeter wave systems and the like, and does not disclose analog and mixed signal systems, as is recited in claims 2 - 7, 9, 15 – 18.

Microwave and analog and mixed signal systems are different technologies, and, as such, microwave design techniques cannot be transferred to analog and mixed signal design techniques. Microwave, and analog and mixed signal transmission line topologies are also different topologies and are not transferable.

Microwave operates at a very narrow bandwidth, around a single frequency. For optimal performance, microwave transmission line wires are matched at 50 ohms and work within the narrowly defined bandwidth. Outside of this bandwidth, the resultant reflections distort the signal.

Analog and mixed signal systems operate along a very wide bandwidth, from the direct current that is zero frequency to the ultra high frequency of 100's of Gigahtz. It is not possible to use a microwave transmission line for such analog and mixed signal circuits because the resulting reflections would make the signal unusable.

Thus, Chao does not teach "designing one or more transmission lines for analog and mixed signal circuit design", as recited in currently amended claim 2, or "analog and mixed signal transmission lines" as recited in currently amended claim 6. Applicants respectfully submit that currently amended claims 2, 6, 15 and 17 are allowable over Chao et al. and claims 3 – 5, 7, 9, 16, and 18, dependent therefrom, are also allowable over Chao et al.

Pileggi et al.

Claim 6 has been rejected under 35 U.S.C. 102(e) as being anticipated by Pileggi et al. (US patent 6,286, 128). Applicants respectfully traverse the Examiner's rejection.

Pileggi discloses digital technology and time delay design optimizations. Time delay solutions depend mainly on wire placement methods. Pileggi states [col. 2, l 67; col. 3, ll 1 – 2], "The logic optimization and placement are preformed such that the interconnect with a predictable delay is concurrently placed with the logic circuitry".

Additionally, since Pileggi disclosures only digital technology, he does not discuss or mention optimizations concerned with signal integrity. The method and apparatus of Pileggi is not applicable and would not work in an analog and mixed signal circuit, wherein the concerns are for both time delay and signal integrity. The arguments as applicable to Luk apply herein.

Thus, Applicants respectfully submit that Pileggi does not disclose an "analog and mixed signal transmission line" and therefore, claim 6 is allowable over Pileggi.

Boyle et al.

Claims 6, 15 and 17- have been rejected under 35 U.S.C. 102(e) as being anticipated by Boyle et al. (US patent 6,557,145). Applicants respectfully traverse the Examiner's rejection.

Boyle discloses digital technology and time delay design optimizations and wire placement methods. The argument provided hereinabove with respect to Pileggi holds for Boyle.

The method and apparatus of Boyle is not applicable and would not work in an analog and mixed signal circuit, where the concerns are both time delay and signal integrity. The arguments as applicable to Luk apply herein.

Thus, Applicants respectfully submit that Boyle does not disclose an "analog and mixed signal transmission lines" as recited in claim 6, or "an analog and mixed signal integrated circuit" as recited in claims 15 and 17. Claim 6, 15 and 17 are therefore allowable over Boyle.

Dansky et al

Claims 2 – 13, 15 – 18, 23 – 24 and 26 – 28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Dansky et al. (US patent application 6,342,823). Applicants respectfully traverse the Examiner's rejection.

Dansky does not have a design tool; Dansky discloses an "analysis tool, ... based on the net topology obtained from actual product chip layout, the tool transfers..." [col. 3, lines 36-49]. See also col.5, lines 18-36, "Fig. 10 shows the schematic of the analysis tool". As noted, after the chip logic is designed, and the circuits are interconnected, and the wiring layout is obtained, only then are the critical nets identified. Applicants further note Dansky's claim 1:"providing a wiring plan for an integrated circuit having interconnected circuits and transmission lines; identifying a group of constituent parts of the integrated circuit..."

As such, the tool of Dansky is used for analysis after the chip layout is complete and not for designing transmission lines. Thus, Dansky does not disclose "means for designing ..." as recited in claim 2, or "a design topology" as recited in claim 6, or "designing ..." as recited in claim 15, or "a computer softer circuit design product..." as recited in claim 17, "a method for designing ..." as recited in claim 30, or "a method for designing " as recited in claim 32.

Applicants respectfully submit that claims 2, 6, 15, 17, 30 and 32 are allowable over Dansky and claims 3 – 5, 7 - 13, 16, 18, and claims 36 – 41 dependent therefrom, are allowable over Dansky.

Applicants believe that the above amendments and remarks are fully responsive to all the objections and grounds of rejections by the Examiner. In view of the foregoing amendments and remarks, the Applicants respectfully submit that all the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fee associated with this paper to deposit account No. 09-0468.

Respectfully submitted,

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